Amendments to the Claims:

This listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. - 34. (Canceled)

35. (Previously Presented) A method for generating an address value for addressing a memory which is an interleaver or deinterleaver memory, comprising the steps of:

generating a plurality of address fragments;

comparing only a fraction of the generated address fragments with a maximum allowable value;

wherein generating a plurality of address fragments further comprises the step of generating a first address fragment for a first address value, and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

wherein the step of comparing only a fraction of the generated address fragments with a maximum allowable value further comprises the step of comparing only every other address fragment of the plurality of address fragments with the maximum allowable value, whereby the step of comparing comprises comparing the first address fragment with the maximum allowable value.

36. (Previously Presented) The method according to claim 35, further comprising the steps of:

discarding the compared address fragment if it exceeds the maximum allowable value; and

accepting the compared address fragment otherwise.

37. (Previously Presented) The method according to claim 35, wherein the address fragments to be compared are permuted prior to the step of comparing.

38. (Previously Presented) The method according to claim 35, further comprising the step of appending at least one most significant bit(s) to any address fragment or a permuted address fragment.

39. (Previously Presented) The method according to claim 35, wherein the compared address fragment is an odd address fragment to which a 1 is to be appended as a most significant bit.

40. (Previously Presented) The method according to claim 35, wherein an even address fragment is generated in response to a step of discarding or accepting the compared address fragment.

41. (Previously Presented) The method according to claim 35, further comprising the steps of:

generating at least the odd address fragment to be compared and a following even address fragment during a first clock cycle;

if the compared odd address fragment is discarded, outputting the even address fragment during the first clock cycle;

if the compared odd address fragment is accepted, outputting the odd compared address fragment and retaining values of registers of a shift register during the first clock cycle; and

outputting the even address fragment during a second clock cycle following the first clock cycle.

42. (Previously Presented) The method according to claim 41, comprising the step of generating a next odd address fragment; and inputting the next odd address fragment into registers of a shift register.

43. (Previously Presented) The method according to claim 42, wherein the next even and next odd address fragments are generated by means of a feedback function (g(x)).

44. (Previously Presented) The method according to claim 41, wherein the next even and next odd address fragments are generated by means of a feedback function (g(x)).

45. (Previously Presented) The method according to claim 35, further comprising the steps of generating a next odd address fragment; and inputting the next odd address fragment into registers of a shift register.

46. (Previously Presented) The method according to claim 35, further comprising the steps of:

discarding the compared address fragment if it exceeds the maximum allowable value;

accepting the compared address fragment otherwise; and

permuting the generated address fragments, wherein the address fragments to be compared are permuted prior to the step of comparing.

47. (Previously Presented) The method according to claim 46, further comprising the step of appending at least one most significant bit(s) to any address fragment or permuted address fragment.

48. (Previously Presented) The method according to claim 47, wherein the compared address fragment is an odd address fragment to which a 1 is to be appended as a most significant bit.

49. (Previously Presented) The method according to claim 48, wherein an even address fragment is generated in response to discarding or accepting the compared address fragment.

50. (Previously Presented) A method for generating an address value for addressing a memory which is an interleaver or deinterleaver memory comprising the steps of:

generating a plurality of address fragments by generating a first address fragment for a first address value and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

comparing only a fraction of the generated address fragments by comparing only every other address fragment of the plurality of address fragments with stored address fragments, which are known to be out of range when permuted and comparing the first address of fragment with the stored address fragments.

51. (Previously Presented) The method according to claim 50, further comprising the step of permuting the generated address fragments after the step of comparing.

52. (Previously Presented) A device for generating address values for addressing a memory, which is an interleaver or deinterleaver memory, comprising:

a means for generating a plurality of address fragments configured to generate a first address fragment for a first address value and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

a comparator means configured to compare only a fraction of the plurality of address fragments with a maximum allowable value and further configured to compare only every other address fragment of the plurality of address fragments with the maximum allowable value and thereby to compare the first address fragment with the maximum allowable value.

53. (Previously Presented) The device according to claim 52, further comprising a selector means configured to discard the compared address fragment if it exceeds the maximum allowable value, and to accept the compared address fragment otherwise.

54. (Previously Presented) The device according to claim 52, further comprising a permuting means configured to permute the address fragments, the permuting means being provided prior to the comparator means.

55. (Previously Presented) The device according to claim 52, further comprising a toggle means configured to append at least one most significant bit(s) to any address fragment, or to any permuted address fragment, in order to generate the address value.

56. (Previously Presented) The device according to claim 52, wherein the compared address fragments are address fragments to which a 1 is to be appended as a most significant bit.

57. (Previously Presented) The device according to claim 52, wherein the means for generating address fragments is configured to generate a next even address fragment in response to a discarding or acceptance of the compared address fragment.

58. (Previously Presented) The device according to claim 52, wherein the means for generating address fragments further comprises:

a shift-register comprising a predetermined number of registers configured to generate address fragments to be compared during a first clock cycle;

an address fragment calculation means configured to generate a next even address fragment during the first clock cycle, which is based on the address fragment to be compared;

a selector means is configured to, if the compared address fragment is discarded, output the even address fragment in response to a first control signal (M) during the first clock cycle, and to output the compared address fragment during the first clock cycle if the compared address fragment is accepted, and to output the even address fragment during a second clock cycle following the first clock cycle; and

the shift register is configured to retain present values of the registers during the first clock cycle in response to a second control signal (E) if the compared address fragment is accepted.

59. (Previously Presented) The device according to claim 52, wherein the device is implemented by software comprising readable program means to be run by a processor.

60. (Previously Presented) The device according to claim 52, wherein the device is implemented as an application specific integrated circuit.

61. (Previously Presented) The device according to claim 52, wherein the device is implemented as a field programmable gate array.

62. (Previously Presented) The device according to claim 52, further comprising a shift register configured to generate a maximum length pseudo noise sequence.

63. (Previously Presented) The device according to claim 52, further comprising

a selector means configured to discard the compared address fragment if it exceeds the maximum allowable value, and to accept the compared address fragment otherwise; and

a permuting means configured to permute the address fragments, the permuting means being provided prior to the comparator means.

64. (Previously Presented) The device according to claim 63, further comprising toggle means configured to append at least one most significant bit(s) to any address fragment, or permuted address fragment, in order to generate the address value.

65. (Previously Presented) The device according to claim 64, wherein the compared address fragments are address fragments to which a 1 is to be appended as a most significant bit.

66. (Previously Presented) The device according to claim 65, wherein the means for generating address fragments is configured to generate a next even address fragment in response to discarding or accepting the compared address fragment.

67. (Previously Presented) The device according to claim 65, wherein the means for generating address fragments further comprises:

a shift-register comprising a predetermined number of registers configured to generate address fragments to be compared during a first clock cycle;

address fragment calculation means configured to generate a next even address fragment during the first clock cycle, which is based on the address fragment to be compared;

the selector means is configured to, if the compared address fragment is discarded, output the even address fragment in response to a first control signal (M) during the first clock cycle, and to output the compared address fragment during the first clock cycle if the compared address fragment is accepted, and to output the even address fragment during a second clock cycle following the first clock cycle; and

the shift register is configured to retain present values of the registers during the first clock cycle in response to a second control signal (E) if the compared address fragment is accepted.

68. (Previously Presented) The device according to claim 67, wherein the address fragment calculation unit mean is configured to generate a next odd address fragment, based on the even address fragment, and feed back said next odd address fragment to the shift register.

69. (Previously Presented) The device according to claim 68, wherein the address fragment calculation means is configured to generate the next even and next odd address fragments by means of a feedback function.

70. (Previously Presented) The device according to claim 69, wherein the device is implemented as an application specific integrated circuit.

71. (Previously Presented) The device according to claim 69, wherein the device is implemented as a field programmable gate array.

72. (Previously Presented) The device according to claim 71, further comprising a shift register configured to generate a maximum length pseudo noise sequence.

73. (Previously Presented) The device according to claim 67, wherein the address fragment calculation means is configured to generate the next even and next odd address fragments by means of a feedback function

74. (Previously Presented) The device according to claim 73, wherein the device is implemented by software comprising readable program loaded in a computer readable medium and executed by a processor.

75. (Previously Presented) A device for generating address values for addressing a memory which is an interleaver or deinterleaver memory, comprising:

a means for generating a plurality of address fragments configured to generate a first address fragment for a first address value and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

a comparator means configured to compare only a fraction of the plurality of address fragments with a maximum allowable value, further being configured to compare only every other address fragment of the plurality of address fragments with stored address fragments, which are known to be out of range when permuted, and thereby to compare the first address fragment with stored address fragments.

76. (Previously Presented) The device according to claim 75, further comprising a permuting means configured to permute the address fragments, the permuting means being provided after the comparator means.

77. (Previously Presented) An interleaver for interleaving a block of data, having a memory which is an interleaver memory in combination and a device for generating address values, comprising:

a means for generating a plurality of address fragments, and comparator means configured to compare only a fraction of the plurality of address fragments with a maximum allowable value, the means for generating a plurality of address fragments being configured to generate a first address fragment for a first address value and a second address fragment, which is consecutive of the first address fragment, for a second address value, and the comparator means being configured to compare only every other address fragment of the plurality of address fragments with the maximum allowable value and thereby compare the first address fragment with the maximum allowable value.

78. (Previously Presented) A deinterleaver for interleaving a block of data, having a memory, which is a deinterleaver memory, and a device for generating address values for addressing the memory, comprising:

a means for generating a plurality of address fragments, and comparator means configured to compare only a fraction of the plurality of address fragments with a maximum allowable value, the means for generating a plurality of address fragments being configured to generate a first address fragment for a first address value and a second address fragment, which is consecutive of the first address fragment, for a second address value, and the comparator means being configured to compare only

every other address fragment of the plurality of address fragments with the maximum allowable value and thereby compare the first address fragment with the maximum allowable value.

79. (Previously Presented) A communication apparatus for communicating data, comprising a memory which is an interleaver memory or a deinterleaver memory, and a device for generating address values for addressing the memory, comprising:

a means for generating a plurality of address fragments configured to generate a first address fragment for a first address value and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

a comparator means configured to compare only a fraction of the plurality of address fragments with a maximum allowable value configured to compare only every other address fragment of the plurality of address fragments with the maximum allowable value and thereby compare the first address fragment with the maximum allowable value.

80. (Previously Presented) The communication apparatus according to claim 79, wherein the communication apparatus is one selected from the group consisting of a mobile radio terminal, a pager, a communicator, an electronic organizer, and a smartphone.

81. (Previously Presented) The communication apparatus according to claim 79, wherein the communication apparatus comprises a mobile telephone.

82. (Previously Presented) A communication apparatus for receiving data, comprising:

a deinterleaver with a memory;

a device for generating address values for addressing the memory;

a means for generating a plurality of address fragments being configured to generate a first address fragment for a first address value and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

a comparator means configured to compare only a fraction of the plurality of address fragments with a maximum allowable value, the comparator means further being configured to compare only every other address fragment of the plurality of

address fragments with the maximum allowable value and thereby to compare the first address fragment with the maximum allowable value.

83. (Previously Presented) The communication apparatus according to claim 82, wherein the communication apparatus is one selected from the group consisting of a set-top-box, a television set, and a mobile television receiver.

84. (Previously Presented) A software program product embodied on a computer readable medium executable by computer hardware when the product is executed by a processor contained in said computer hardware, the product having instructions comprising:

generating an address value for addressing a memory which is an interleaver or deinterleaver memory;

generating a plurality of address fragments, and comparing only a fraction of the generated address fragments with a maximum allowable value;

when generating a plurality of address fragments, generating a first address fragment for a first address value, and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

when comparing only a fraction of the generated address fragments with a maximum allowable value, comparing only every other address fragment of the plurality of address fragments with the maximum allowable value, whereby the step of comparing comprises comparing the first address fragment with the maximum allowable value.